

An Efficient VLSI Architecture for Discrete Wavelet Transform

¹Chih-Hsien Hsia*, ¹Jia-Hao Yang, and ²Weihua Wang

¹Department of Electrical Engineering
Chinese Culture University, Taipei, Taiwan

Email: chhsia625@gmail.com

²College of Foreign Languages
Taiyuan University of Technology, China

Email: 771010633@qq.com

Abstract— A Lifting-based Discrete Wavelet Transform (DWT) is a time/frequency analysis conversion method that is often used in JPEG2000 image compression systems. Its filter bank has a dual-mode base function that consists of coefficients of 9/7 and 5/3. Generally, in the process of realizing Very Large Scale Integration (VLSI) architecture, there is a longer critical path and increased cost of hardware, so paper proposes a folding and pipelined architecture to solve the problems in VLSI architecture design; In order to solve the problem of a large area of hardware due to the excessive use of the multipliers in dual-mode operation, a shifter-adder-multiplier architecture and dual-mode filter architecture are combined. The experimental results show that the hardware architecture proposed in this work has a short critical path. The hardware supports dual-mode hardware wavelet coefficients, decrease latency, and multiplierless, and more suitable for VLSI to implement and apply in low cost JPEG2000 compression systems.

I. INTRODUCTION

The Discrete Wavelet Transform (DWT) has been widely used in different fields, including image processing, data compression, computer vision, speech processing, numerical analysis, signal analysis, biometric recognition and biological medicine, etc. By using multiresolution, time or a spatial domain is transformed to a frequency domain. In recent years, many works have improved the VLSI architecture of 1-D lifting-based DWT's. Hsieh et al. proposed [1] a lifting-based 5/3 discrete wavelet filter VLSI architecture that used three-stage pipeline architecture to reduce the critical path and latency. However, its structure can only deal with a 5/3 integer point filter so it is limited in its application. In [2], the structure of a parallel distributed arithmetic with the function of a multiplier and accumulator allows easier realization of the VLSI architecture; nevertheless, the structure used a Look-Up Table (LUT) to replace multiplier, which is more expensive. The LUT requires more memory space, which impacts the VLSI hardware structure's cost and area.

Faced with the efficiency of a multiplier, Sowjanya *et al.* [4] used pipelined architecture for lifting-based 9/7 wavelet filters to reduce the hardware area and to increase the throughput of the output signals. The work used a five stage pipelined architecture and shared computing resources between different stages to maximize the capability of the VLSI hardware. However, multi-stage pipeline architecture also involves too many registers and multipliers and has a long

critical path. Liao *et al.* [5] proposed a recursive combined with dual scan architecture, which, uses the independent relationship between 1-D recursive to alternate non-overlapping wavelet coefficients in a clock cycle and dual scan architecture to share two independent data and hardware to give better performance. The circuit had too many control units and needed more registers. In [6] a folding architecture to dual-mode was used to enhance the DWT to allow VLSI architectures to achieve greater hardware utilization but the area of the hardware is increased. In [7], because of the nature of a wavelet orthogonal. A multiplier and adder transform between different levels in order to increase the processing speed. The result is greater speed but the area is also increased. It is less applicable in a low-cost embedded system platform. As stated in previous works, although many methods have been proposed to increase the efficiency and decrease the processing time for VLSI hardware, the number of operators, the hardware area and the critical path could be improved significantly. This paper uses a 1-D dual-mode lifting-based DWT (9/7 and 5/3 wavelet coefficients filter) with VLSI hardware consolidation to increase its potential applications, regarding the critical path that is a result using a multiplier and uses a shift and adder method to replace the multiplier and reduce the number of multipliers to increase the speed. At the same time, for the low hardware rate problem that is associated with VLSI hardware architectures is addressed by using the folding pipelined VLSI architecture is designed to enhance its the efficiency of the hardware, in order to allow its use in low-cost embedded platforms.

In Section II illustrates the proposed architecture of VLSI hardware and its analysis. Section III compares the proposed architecture and previous works. Conclusions are drawn in Section IV.

II. VLSI ARCHITECTURE AND ITS IMPLEMENTATION FOR THE 1-D DUAL-MODE LIFTING-BASED DWT

This section presents the VLSI architecture and discusses the concept of the three VLSI architecture designs for the circuit. These are 1) A pipeline architecture design, 2) A shift and adder architecture design, and 3) A folding architecture design.

A. Pipeline Architecture Design

The principle of pipeline architecture divides the computing program's execution for a few steps and separates hardware into several stages, as appropriate. Each stage implements the individual steps of different computing programs synchronously to achieve overlapping execution by a computing program. However, the use of overlapping execution of a computing program to increase the output signal reduces the execution time for a single computing program.

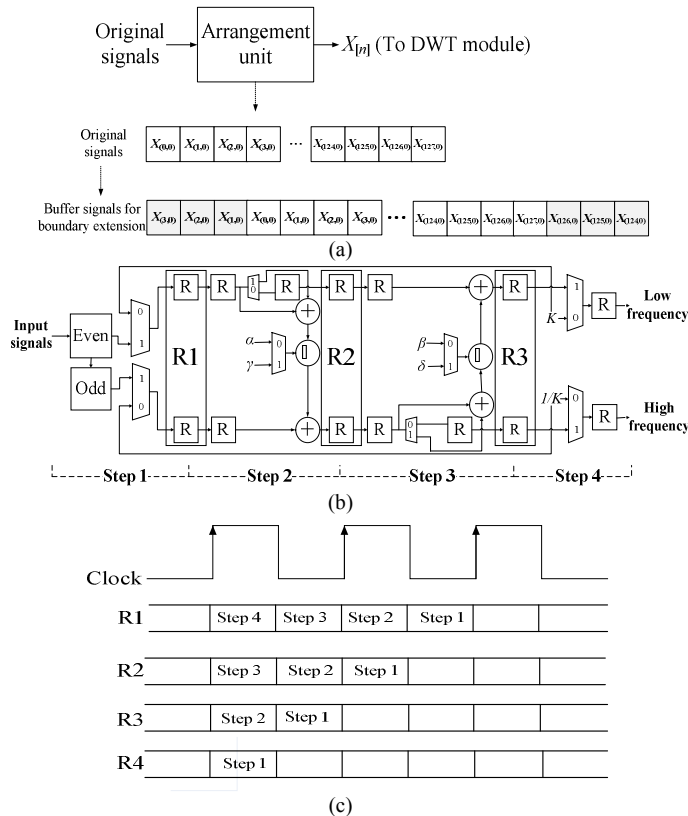


Fig. 1. The VLSI architecture diagram of the proposed 1-D dual-mode lifting-based DWT: (a) Mirror mapping approach to handle the edge after re-ordering process(Input signal arrangement unit for boundary extension). (b) Three pipeline architecture for 1-D DWT. (c) Clock table.

Before entering DWT module operation, a mirror mapping process to deal with boundary extension [8] so that the JPEG2000 compression system can be used. When the serial signal from the horizon is read, those signals are reordered in accordance with the principle of specular mapping and the reordered messages are sent to the pipeline architecture, as shown in Fig. 1(a). The dual-mode filter with 9/7 and 5/3 wavelet coefficients can switch its mode according to the needs of the application. The improved architecture in Fig. 1(b) calculates its input signal (even or odd) and returns its output signal to the input. The next even or odd original input signal is calculated in sequence. In this way, traditional VLSI architecture hardware area is reduced in areas by 50% by adding the pipeline infrastructure and folding architecture. No additional control of the input signal is needed to select the correct coefficient path. Figure 1(b) shows different processing of registers at the same time. In the time table of

pipeline processing, work at every level is connected without conflict and is orderly and separate so the entire circuit hardware is faster. As shown in Fig 1(c), R1, R2, and R3 are pipelines in three different stages and can also be treated as a register, to ensure the correctness of the values. This synchronizes the finishing time for all pipelines and ensures that pipelines at different stages deliver to the next stage synchronously after all pipelines have finished calculations, which ensures that every stage's output value are accurate.

B. Shift and Adder Architecture Design

The hardware cost and performance of multipliers have been problems for a long time. Therefore, this paper presents a shift and adder architecture that solves the hardware problem of a multiplier. In the lifting-based DWT, either 9/7 or 5/3 filter coefficients can be used in a dual-model architecture. If a binary value shift right one bit, it is divided by two because of its binary relationship. If a binary value shifts left one bit, it will be multiple by two because of its binary relationship itself. Such a shift can have the square of two effect and using an adder to add the shifted values removes the need for a multiplier.

In the architecture designed by this work, the input signal is 8 bits and the output signal is 16 bits. The first bit is sign bit and the ten bits in the middle are integer bits. The last five bits are fraction parts [8]. In order to calculate the fraction part, the 8 bit input signal for the architecture is shifted left by 5 bits, which is 2^5 . It then shifts right 5 bits and is divided into 2^5 so amplified signal has 5 bits of space to calculate the fraction part and feed back to the original signal value, which is maintained so that the middle value has 5 bits of space to calculate the fraction part calculation the signal errors in the output are reduced.

The work proposes a shift and adder architecture to replace a wavelet multiplier coefficient α of the original 9/7 wavelet filter bank, as shown in Fig. 2(a). If the input signal is x , when it has entered the proposed VLSI architecture, x can have two paths: on one path x shifts right one bit (It is divided by two and becomes $0.5x$) and on the other path x plus $0.5x$ become $1.5x$ and becomes negative in sign so the output is $-1.5x$ (-1.5 is the α coefficient that is produced by hardware), which is close to the theoretical wavelet coefficient of -1.586 . As shown in Fig. 2(b), the multiplier coefficients α of the original 9/7 wavelet filter bank are also replaced by a shift and adder architecture; If the input signal is y , when it enters the proposed VLSI architecture, y shifts right 4 times and the sign become negative, so the output becomes $-0.062y$ (-0.062 is the β coefficient that is produced by the hardware), which is close to the theoretical wavelet coefficient of -0.053 . This process is repeated (see Fig. 2(c) - (f)), The coefficient is 0.799 , which is close to the theoretical wavelet coefficient of 0.883 ; the coefficient is 0.468 , which is close to the theoretical wavelet coefficient of 0.444 . The adjustment coefficient is made before the output, the K wavelet coefficient is 1.25 , which is close to the theoretical coefficient of 1.230 and the $1/K$ coefficient is 0.8125 , which is close to the theoretical wavelet coefficient of 0.813 . All of the proposed methods achieve a

relatively good trade-off between hardware limitations and the signal quality of VLSI [8].

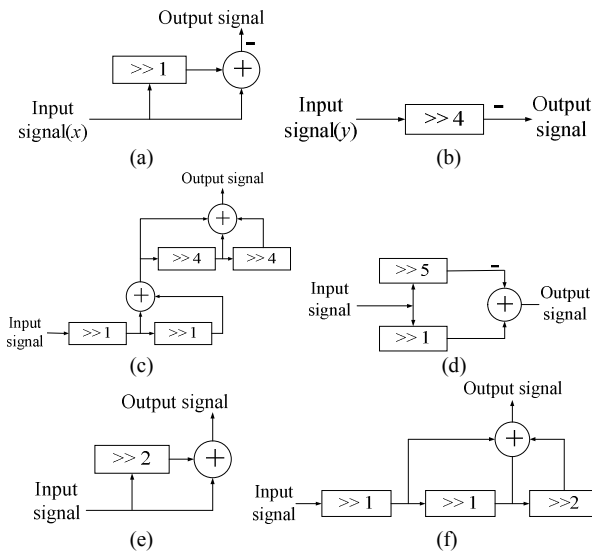


Fig. 2. The hardware implementations of the six coefficients of the 9/7 filter: (a) α . (b) β . (c) γ . (d) δ . (e) K . (f) $1/K$.

C. Folding Architecture Design

The Conventional lifting-based DWT coefficients include 5/3 and 9/7 filter banks. This work uses four coefficients α , β , γ , and δ , for a 9/7 filter and two coefficients α and β , for a 5/3 wavelet filter. The folding architecture design reduces the area and the performance. However, in the 9/7 wavelet filter, the coefficients, α , β , γ , and δ are all similar architectures and they are not in conflict when processing at the same time, so using the folding principle simplifies a 9/7 wavelet filter coefficient into α and β which is a group of arithmetic circuits and γ and δ as a group of arithmetic circuits. A selective line is also used to choose different coefficients.

In Fig. 3, the input signal is divided into an even signal and an odd signal. R3_E is an even signal that is feedback to input after processed by a third level pipeline treatment; R3_O is an odd signal, will also be feedback to the input after processed by a third class pipeline treatment. When the clock is at 1, the original even signal is input and calculated; When the clock is at 0, the original odd signal is input and calculated. It can be achieved to complete high-frequency signal and low-frequency signals are output in two clock cycles.

Figure 4 combined the dual-mode lifting-based coefficient with the VLSI architecture design. Two signal lines are control units for the selection of wavelet coefficients for a 9/7 filter or a 5/3 filter. In fact, when the clock is at 1, α and β begin to work and clock is at 0, γ and δ begin to work. Because after α and β combined with γ and δ , the two coefficients work with different clocks, so they share one adder. However, the number of adders in use can be reduced, so the hardware performance is enhanced as a whole by not using a multiplier. For example, according to Fig. 4(a) combined 5/3 and 9/7 wavelet coefficients use the circuit in

Fig. 2(a) and Fig. 2(c) and a multiplexer is added as the 5/3 for 9/7 filter bank functions.

When the folding dual-mode filter is selected, three of the original adders go through α and γ coefficients, but the folding architecture allows the coefficients to share an adder so the combined wavelet coefficients only need to use two adders, which saves the hardware resources of the adders. In addition, because the proposed architecture have a wordlength effect in the floating part, a more accurate result is close to zero after the shift right. For example, if the input is 8 bits, the shift is more than 8 bits to the right. The data that approaches zero is meaningless, so in the improved folding dual-mode filter, the banks remove a floating part that is too precise by shifting it right.

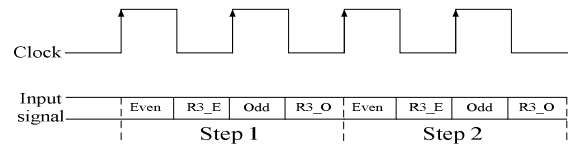


Fig. 3. Clock reuse assigned from modified folding architecture.

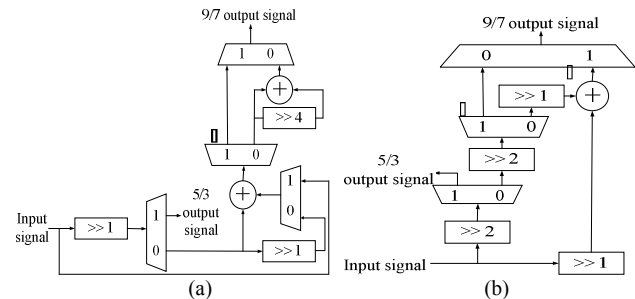


Fig. 4. Folding dual-mode shift wavelet coefficients of VLSI architecture: (a) Combined α and γ for 5/3 and 9/7 filters. (b) Combined β and δ for 5/3 and 9/7 filters.

III. EXPERIMENTAL RESULTS AND COMPARISONS

This paper designed a VLSI architecture for a 1-D dual-mode lifting-based DWT, that uses VerilogHDL and Xilinx ISE for functional simulation. When the input signal is 8 bits, in order to increase the accuracy of information, the shift register between the input and the output has 11 bits and a fraction part of 5 bits. So the output wordlength is a 16 bits wavelet signal [8]. Finally, a Xilinx FPGA chip is used to test the XC3S200AN of a Spartan3A series.

Several 1-D lifting-based DWT VLSI architectures are compared and the quantities of adders, multipliers, and multiplexers are listed in Table 1. The proposed architecture does not use any multiplier and the critical path delay between the input and the output is 8Ta. This allows a greater increase in speed for a 1-D 9/7 lifting-based filter because multipliers occupy more hardware resources and delay the finishing time so there is excessive latency. The analysis shows that multipliers, registers and multiplexers are widely used in [4] and [5] to achieve high performance for the hardware, which results in a greater hardware cost than that for work, in terms of the quantities of adders and multipliers. Nevertheless, Cooklev [7] proposed an orthogonal structure in which every

level needs four adders and two multipliers so N levels require $2N + 2N$ adders $N + 1$ and multipliers. This system also uses more multipliers, adders and critical paths.

Finally, the original signal is compressed before transmission while the video and image input signal requires too much time and results in a delay at the transmission side, so in the related works [3-7], [11-13], the critical path time is relatively important (the delay in transmission is the main restriction in the overall architecture computing efficiency) in VLSI architecture, as shown in Table 2.

TABLE 1. COMPARISONS OF ONE-LEVEL 1-D ARCHITECTURES FOR LIFTING-BASED DWT.

Proposed	Adder	Multiplier	Multiplexer
Sowjanya <i>et al.</i> [4] (9/7 filter)	8	6	0
Liao <i>et al.</i> [5] (9/7 filter)	8	6	6
Martina <i>et al.</i> [6] (9/7 filter)	11	0	11
Cooklev [7] (5/3 filter)	$2N+2$	$N+1$	5
Tsai <i>et al.</i> [11] (9/7 filter)	18	9	0
Tian <i>et al.</i> [12] (9/7 filter)	8	5	0
Souani <i>et al.</i> [13] (9/7 filter)	4	4	0
This work (Dual-mode filters)	9	0	For 9/7 = 9 For 5/3 = 2

* Suppose the input signal is of size N

TABLE 2. PERFORMANCE COMPARISONS OF VARIOUS 9/7 1-D LDWT HIGH THROUGHPUT ARCHITECTURES.

Proposed	Critical Path Delay
Sowjanya <i>et al.</i> [4] (9/7filter)	$8T_a+6T_m$
Martina <i>et al.</i> [6] (9/7 filter)	$11T_a$
Cooklev [7] (5/3 filter)	$(4N)T_a+(2N)T_m$
Tsai <i>et al.</i> [11] (9/7 filter)	$4T_a+6T_m$
Tian <i>et al.</i> [12] (9/7 filter)	$8T_a+5T_m$
This work (Dual-mode filters)	$8T_a$

* T_m : Multiplier operation time; T_a : Adder operation time.

IV. CONCLUSIONS

This paper addresses the architecture problems of a conventional 1-D lifting-based DWT, by addressing the problems of the arithmetic unit, the single mode filter coefficients and the hardware processing time, etc. This work presents pipeline architecture and folding architecture to address these issues in a 1-D dual-mode (supporting 5/3 lossless and 9/7 lossy coding) Lifting-based Discrete Wavelet Transform (LDWT). Due to the regularity and simplicity of the DWT architecture, a dual-mode 1-D LDWT prototyping Xilinx FPGA chip is designed using a XC3S200AN of the Spartan3A series. As results, show that the architecture does

not need any multiplier and only needs an 8Ta critical path. With 5.2ns latency, 3.1mV power consumption and 93.2MHz operating frequency, it is a low-resource, low-power and high efficiency hardware architecture that is suitable for future use in low-cost embedded platforms.

ACKNOWLEDGMENT

The authors would like to thank the anonymous reviewers of their paper for the many helpful suggestions. This work was supported by the Chinese Culture University, Taiwan.

REFERENCES

- [1] C.-F. Hsieh, T.-H. Tsai, N.-J. Hsu, and C.-H. Lai, "A novel, efficient architecture for the 1D, lifting-based DWT with folded and pipelined schemes," *Joint Conf. on Information Sciences*, 2006.
- [2] A. M. Al-Haj, "An FPGA-based parallel distributed arithmetic implementation of the 1-D discrete wavelet transform," *Informatica*, vol. 29, no.1, pp. 241–247, 2005.
- [3] C.-H. Hsia, "A new VLSI architecture for symmetric mask-based discrete wavelet transform," *J. of Internet Technology*, vol. 15, no. 7, pp. 1083–1090, 2014.
- [4] D. Sowjanya, K. N. H. Srinivas, and P. V. Ganapathi, "FPGA implementation of efficient VLSI architecture for fixed point 1-D DWT using lifting scheme," *Int. J. of VLSI design & Communication Systems*, vol.3, no.4, pp. 37–48, 2012.
- [5] H. Liao, M. K. Mandal, and B. F. Cockburn, "Efficient architectures for 1-D and 2-D lifting-based wavelet transforms," *IEEE Trans. on Signal Processing*, vol. 52, no. 5, pp. 1315–1326, 2004.
- [6] M. Martina and G. Masera, "Folded multiplierless lifting-based wavelet pipeline," *Electronics Letters*, vol. 43, no. 5, pp. 27–28, 2007.
- [7] T. Cooklev, "An efficient architecture for orthogonal wavelet transforms," *IEEE Signal Processing Letters*, vol. 13, no. 2, pp. 77–79, 2006.
- [8] C.-H. Hsia, J.-S. Chiang, and J.-M. Guo, "Memory-efficient hardware architecture of 2-D dual-mode lifting-based discrete wavelet transform," *IEEE Trans. on Circuits and Systems for Video Technology*, vol. 23, no. 4, pp. 671–683, 2013.
- [9] I. Daubechies, and W. Sweldens, "Factoring wavelet transforms into lifting steps," *J. of Fourier Analysis and Application*, vol. 4, no. 3, pp. 247–269, 1998.
- [10] C.-H. Hsia, J.-M. Guo, and J.-S. Chiang, "Improved low-complexity algorithm for 2-D integer lifting-based discrete wavelet transform using symmetric mask-based scheme," *IEEE Trans. on Circuits and Systems for Video Technology*, vol. 19, no. 8, pp. 1201-1208, 2009.
- [11] C.-F. Tsai, H.-S. Wang, K.-C. Hung, and S.-C Hsia, "Non-recursive discrete periodized wavelet transform using segment accumulation algorithm and reversible round-off approach," *IEICE Trans. on Information and Systems*, vol. E91–D, no. 11, pp. 2666–2674, 2008.
- [12] X. Tian, Z. Zhou, Y.-H. Tan, and J.-W. Tian, "Parallel 9/7-tap wavelet based on lifting structure," *Electronics Letters*, vol. 43, no. 11, pp. 617–618, 2007.
- [13] C. Souani, M. Abid, K. Torki, and R. Tourki, "VLSI design of 1-D DWT architecture with parallel filters," *Integration, the VLSI J.*, vol. 29, no. 2, pp. 181–207, 2000.